RAMAIAH
Institute of Technology

CURRICULUM

for the Academic Year 2021 – 2022

(Batch of 2021 – 2023)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

M. Tech (DIGITAL ELECTRONICS AND COMMUNICATION)

I – IV Semester M. Tech

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
Bangalore – 560054.

About the Institute

Dr. M. S. Ramaiah a philanthropist, founded 'Gokula Education Foundation' in 1962 with an objective of serving the society. M S Ramaiah Institute of Technology (MSRIT) was established under the aegis of this foundation in the same year, creating a landmark in technical education in India. MSRIT offers 17 UG programs and 15 PG programs. All these programs are approved by AICTE. All eligible UG and PG programs are accredited by National Board of Accreditation (NBA). The institute is accredited with **'A^{+}' grade by NAAC in March 2021** for 5 years. University Grants Commission (UGC) & Visvesvaraya Technological University (VTU) have conferred Autonomous Status to MSRIT for both UG and PG Programs since 2007. The institute is a participant to the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. The institute has 380 competent faculty out of which 60% are doctorates. Some of the distinguished features of MSRIT are: State of the art laboratories, individual computing facility for all faculty members, all research departments active with sponsored funded projects and more than 300 scholars pursuing Ph.D. To promote research culture, the institute has established Centre of Excellence for Imaging Technologies, Centre for Advanced Materials Technology, Centre for Antennas and Radio Frequency systems (CARFS), Center for Cyber Physical Systems & Schneider Centre of Excellence. **M S Ramaiah Institute of Technology has obtained "Scimago Institutions Rankings" All India Rank 65 & world ranking 578 for the year 2020.**

The Entrepreneurship Development Cell (EDC) and Section 8 company "Ramaiah Evolute" have been set up on campus to incubate startups. **M S Ramaiah Institute of Technology secured All India Rank 8th for the year 2020 for Atal Ranking of Institutions on Innovation Achievements (ARIIA), by MoE, Govt. of India.** MSRIT has a strong Placement and Training department with a committed team, a good Mentoring/Proctorial system, a fully equipped Sports department, large air-conditioned library with good collection of book volumes and subscription to International and National Journals. The Digital Library subscribes to online e-journals from Elsevier Science Direct, IEEE, Taylor & Francis, Springer Link, etc. MSRIT is a member of DELNET, CMTI and VTU E-Library Consortium. MSRIT has a modern auditorium and several hi-tech conference halls with video conferencing facilities. The institute has excellent hostel facilities for boys and girls. MSRIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association.

As per the National Institutional Ranking Framework (NIRF), MoE, Government of India, M S Ramaiah Institute of Technology has achieved 65th rank among 1143 top Engineering institutions of India for the year 2021 and is 1st amongst the Engineering colleges affiliated to VTU, Karnataka.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST, ISRO and AICTE with funding amount worth Rs.1crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio-economic needs

Mission of the Institute

RIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy for socio-economic needs*

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

Vision of the Department

To evolve into a department of national and international repute for excellence in education and cutting-edge research in the domain of Electronics and Communication Engineering

Mission of the Department

The department will continuously strive to

1. *Provide a world-class learning environment that caters to local and global technological and social requirements*
2. *Initiate research collaborations with academia and industries to perform cutting edge research leading to socio-technological innovations*
3. *Develop skills for pursuing innovation and entrepreneurial ventures for graduating engineers*

Program Educational Objectives (PEOs)

PEO1: *Be successful practicing professionals or pursue doctoral studies in areas related to the program, contributing significantly to research and development activities*

PEO2: *Engage in professional development in their chosen area by adapting to new technology and career challenges*

PEO3: *Demonstrate professional, ethical and social responsibilities of the engineering profession*

Program Outcomes (POs)

PO1: ***Development of Solutions:*** *An ability to independently carry out research / investigation and development work to solve practical problems*

PO2: ***Technical Presentation Skills:*** *An ability to write and present a substantial technical report/document*

PO3: ***Analyze Complex Systems:*** *A practical ability and theoretical knowledge to design and analyze complex electronics based and/or communication systems*

PO4: ***Develop Novel Designs:*** *An ability to apply their in-depth knowledge in electronics and communications domain to evaluate, analyze and synthesize existing and novel designs*

PO5: ***Team Work and Project Management:*** *An ability to effectively participate as a team member and develop project management skills necessary for a professional environment*

CURRICULUM CREDITS DISTRIBUTION

Semester	Professional Courses – Core (Theory & Lab) (PC-C)	Professional Courses – Electives (PC-E)	Technical Seminar (TS)	Project Work/ Internship (PW/IN)	Credits in a semester
First	10	12	2	-	**24**
Second	10	12	2	-	**24**
Third	4	4	-	10	**18**
Fourth	-	-	-	22	**22**
Total	**24**	**28**	**4**	**32**	**88**

SCHEME OF TEACHING

M. Tech (Digital Electronics and Communication)

(Batch 2021 – 2023)

I SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MLC11	Advanced Engineering Mathematics	PS-C	3	1	0	4	5
2.	MLC12	Advanced Digital Communication	PS-C	3	1	0	4	5
3.	MLCExx	Elective 1	PS-E	4	0	0	4	4
4.	MLCExx	Elective 2	PS-E	4	0	0	4	4
5.	MLCExx	Elective 3	PS-E	4	0	0	4	4
6.	MLCL13	Advanced Digital Communication Laboratory	PS-C	0	0	1	1	2
7.	MLCL14	Digital System Design Laboratory	PS-C	0	0	1	1	2
8.	MLC15	Technical Seminar I	TS	0	0	2	2	4
Total				**18**	**2**	**4**	**24**	**30**

II SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MLC21	Wireless Communication	PS-C	4	0	0	4	4
2.	MLC22	Advanced Embedded Systems	PS-C	4	0	0	4	4
3.	MLCExx	Elective 4	PS-E	4	0	0	4	4
4.	MLCExx	Elective 5	PS-E	4	0	0	4	4
5.	MLCExx	Elective 6	PS-E	4	0	0	4	4
6.	MLCL23	Advanced Embedded Systems Laboratory	PS-C	0	0	1	1	2
7.	MLCL24	Advanced Signal and Image Processing Laboratory	PS-C	0	0	1	1	2
8.	MLC25	Technical Seminar II	TS	0	0	2	2	4
Total				**20**	**0**	**4**	**24**	**28**

III SEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MLC31	Multimedia Communication	PC-C	4	0	0	4	4
2.	MLCExx	Elective 7	PC-E	4	0	0	4	4
3.	MLC32	Internship/Industrial Training	IN	0	0	4	4	8
4.	MLC33	Project Work – I	PW	0	0	6	6	12
Total				**8**	**0**	**10**	**18**	**28**

IVSEMESTER

SI. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MLC41	Project Work – II	PW	0	0	22	22	44
Total				**0**	**0**	**22**	**22**	**44**

LIST OF ELECTIVES

SI. No.	Course Code	Course Title	Credits			
			L	T	P	Total
1.	MLCE01	Antenna Theory and Design	4	0	0	4
2.	MLCE02	Digital System Design using HDL	4	0	0	4
3.	MLCE03	VLSI Circuits & Systems	4	0	0	4
4.	MLCE04	Advanced Signal and Image Processing	4	0	0	4
5.	MLCE05	MEMS and Nano Electronics	4	0	0	4
6.	MLCE06	Machine & Deep Learning	4	0	0	4
7.	MLCE07	Internet of Things (IoT)	4	0	0	4
8.	MLCE08	Advanced Computer Networks	4	0	0	4
9.	MLCE09	Error Control Coding	4	0	0	4
10.	MLCE10	Broad Band Wireless Networks	4	0	0	4
11.	MLCE11	Communication System Design using DSP	4	0	0	4
12.	MLCE12	RF and Microwave Circuit Design	4	0	0	4
13.	MLCE13	Simulation, Modeling and Analysis	4	0	0	4
14.	MLCE14	Optical Communication Networks	4	0	0	4
15.	MLCE15	Software Defined Radio	4	0	0	4
16.	MLCE16	ASIC Design	4	0	0	4
17.	MLCE17	Advanced Computer Architecture	4	0	0	4
18.	MLCE18	VLSI Signal Processing	4	0	0	4

ADVANCED ENGINEERING MATHEMATICS

Course Code: MLC11 **Credits: 3:1:0**

Prerequisites: Engineering Mathematics **Contact Hours: 70**

Course Coordinator: Sadashiva V. Chakrasali

UNIT – I

Solving Linear Equations: Introduction, Geometry of linear equations, Solution sets of linear systems, Gaussian elimination, Matrix notation, Inverses, Partitioned matrices, Matrix factorization and determinants

Vector Spaces: Vector spaces and subspaces, Linear independence, Rank, Basis and dimension, Linear transformation, Change of basis

UNIT – II

Eigen Values and Eigen Vectors: Eigen values, Eigen vectors and diagonalization, Eigen vectors and linear transformations

Orthogonality: Orthogonal vectors and subspaces, Projections, Orthogonal bases and Gram – Schmidt orthogonalization

UNIT – III

Orthogonality (Continued): Least squares, Inner product spaces, Diagonalization of symmetric matrices, Quadratic forms and SVD

Continuous Optimization: Optimization using gradient descent, Constrained optimization and Lagrange multipliers, Convex optimization

UNIT – IV

Random Variables: Discrete and continuous random variables, Cumulative distribution function (CDF), Probability Mass Function (PMF), Probability Density Function (PDF), Conditional PMF/PDF, Multiple random variables, Joint CDF/PMF/PDF, Independent/uncorrelated random variables, Moment Generating Functions (MGF)

UNIT – V

Random Processes: Introduction to random processes, Specification of random processes, *n*th order joint PDFs, Independent increments, Stationary increments, Mean and correlation of random processes, Stationary, Wide sense stationary and ergodic processes

Filtering Random Processes: Random processes as inputs to linear time invariant systems, Power Spectral Density, Gaussian processes as inputs to LTI systems, White Gaussian noise

References:

1. Strang. G, "Linear Algebra and its Applications", 4thEdition, Cengage Learning, 2014
2. David C. Lay, "Linear Algebra and its Applications", 3rdEdition, Pearson Education, 2013
3. Stephen Boyd, Lieven Vanden berghe, "Convex Optimization", Cambridge University Press, 2004.
4. Henry Stark, John W. Woods, "Probability and Random Processes with Applications to Signal Processing", 3rdEdition, Prentice Hall, 2002
5. Peyton Z. Peebles, "Probability, Random Variables and Random Signal Principles",4th Edition, TMH, 2007
6. M. P. Deisenroth, A. A. Faisal, C. S. Ong, "Mathematics for Machine Learning", 1st Edition, Cambridge University Press, 2020.

Course Outcomes (COs):

1. Employ linear system and vector space concepts in signal processing and communication (POs: 1, 3, 4)
2. Use eigen values, eigen vectors, diagonalization and SVD in signal processing applications (POs: 1, 3, 4)
3. Apply appropriate optimization techniques for realizing machine learning and signal processing applications (POs: 1, 3, 4)
4. Analyze different random variables and their statistical parameters (POs: 1, 3, 4)
5. Classify various random processes and analyze the nature of output random process of a LTI Systems (POs: 1, 3, 4)

ADVANCED DIGITAL COMMUNICATION

Course Code: MLC12 **Credits: 3:1:0**

Prerequisites: Digital Communication **Contact Hours: 70**

Course Coordinator: T. D. Senthilkumar

UNIT – I

Optimum Receivers for AWGN Channel: Waveform and vector AWGN channels, Optimal detection and error probability for band-limited and power-limited signaling

Digital Communication through Fading Multipath Channel: Frequency-nonselective slowly fading channel, Diversity techniques for fading multipath channel, Signaling over frequency-selective slowly fading channel

UNIT – II

Digital Communication through Band-Limited Channels: Optimum receiver for channels with ISI and AWGN, Linear equalization – peak distortion criterion, MSE criterion, Performance of the MSE equalizer, Decision feedback equalization.

UNIT – III

Adaptive Equalization: Adaptive linear equalizer – zero-forcing algorithm, LMS algorithm, Adaptive decision-feedback equalizer, RLS algorithm for adaptive equalization

UNIT – IV

Multichannel and Multicarrier Systems: Multichannel digital communications in AWGN channels. Orthogonal frequency division multiplexing – modulation and demodulation in an OFDM system, FFT algorithm implementation of an OFDM system, bit and power allocation in multicarrier modulation

UNIT – V

Spread Spectrum Signals for Digital Communications: Direct sequence spread spectrum signals – error rate performance, Effect of pulsed interference, Excision of narrowband interference, Frequency hopped spread spectrum signals – Performance in an AWGN channel, Performance in partial-band interference

References:

1. John G. Proakis and Masoud Salehi, “Digital Communications”, 5th Edition, McGraw Hill, 2008.
2. M. K. Simon, S. M. Hinedi and W. C. Lindsey, “Digital Communication Techniques”, Prentice Hall India, 2012.
3. Andrew J. Viterbi, “CDMA: Principles of Spread Spectrum Communications”, Prentice Hall, USA, 2015.

Course Outcomes (COs):

1. Analyze the performance of band- and power-limited signals in the AWGN and fading channel(POs:1, 3, 4)
2. Apply equalization techniques to minimize the effect of inter symbol interference in multipath fading channel(POs:1, 3, 4)
3. Compare the performance of the parameters convergence rate and accuracy of adaptive equalization algorithms(POs:1, 3, 4)
4. Employ multicarrier and multichannel modulation in modern wireless communication systems (POs:1, 3, 4)
5. Evaluate the performance of DSSS and FH spread spectrum systems (POs:1, 3, 4)

ADVANCED DIGITAL COMMUNICATION LABORATORY

Course Code: MLCL13 **Credits: 0:0:1**

Prerequisites: Microwaves and Digital Communication **Contact Hours: 28**

Course Coordinator(s): Sujatha B. and T.D. Senthilkumar

LIST OF EXPERIMENTS

Antennas

1. Experimental studies of radiation pattern of microstrip Yagi-Uda and dipole antennas
2. Impedance measurements of Horn/Yagi/dipole/Parabolic antennas
3. Calculate the directivity and gain of Horn antenna from the radiation pattern
4. Experimental studies of radiation pattern of microstrip patch antenna
5. (a) Measure the S-parameters of an antenna using Network Analyzer
   (b) Study the characteristics of transmission line using Network Analyzer
6. Calculate the antenna parameters of different types of antenna using Software/Simulation tool

Digital Communication

7. Analyze the performance of Quadrature Amplitude Modulation (QAM) and M-ary Phase Shift Keying (PSK) scheme in AWGN channel, and compare the results with theoretical results
8. Compute Bit Error Rate (BER) for different digital modulation schemes in frequency-flat and slowly varying fading channel
9. Bit error rate analysis of digital communication receivers with Maximal Ratio Combining (MRC) receive diversity in frequency-flat and slowly varying fading channel
10. Bit error rate analysis of digital communication receivers with Equal Gain Combining (EGC) receive diversity in frequency-flat and slowly varying fading channel
11. Simulation of Direct Sequence Spread Spectrum (DSSS) techniques
12. Conduct an experiment for (a) Measurement of numerical aperture and attenuation loss in analog fiber optic link (b) voice and data multiplexing using optical fiber
13. Simulation of digital communication system in AWGN and fading channel environment

References:

1. John D Kraus, Ronald J Marhefka, Ahmad S Khan, "Antennas", 4th Edition, Tata McGraw Hill, 2006.
2. Constantine. A. Balanis, "Antenna Theory Analysis and Design", 2nd Edition, John Wiley, 1997.
3. J. G. Proakis and M. Salehi, "Contemporary Communication Systems using MATLAB", PWS Publishing Company, 2007.
4. Cory L Clark, "Labview Digital Signal Processing and Digital Communications", 1st Edition, McGraw Hill Education, Reprint 2014

Course Outcomes (COs):

1. Plot the radiation pattern of different types of antennas. (POs: 1, 3, 4,5)
2. Determine the parameters like gain, beam width and directivity of antennas. (POs: 1, 3, 4,5)
3. Design an antenna array and find the various parameters like directivity and gain by plotting the radiation pattern using software/simulation tool. (POs: 1, 3, 4, 5)
4. Analyze the performance of the digital modulation receivers in AWGN channel. (POs: 1, 3,4,5)
5. Analyze the performance of the digital modulation receivers in fading channel. (POs: 1, 3, 4,5)

DIGITAL SYSTEM DESIGN LABORATORY

Course Code: MLCL14 **Credits: 0:0:1**

Prerequisites: Digital Electronics **Contact Hours: 28**

Course Coordinator: S. L. Gangadharaiah

LIST OF EXPERIMENTS

Using Verilog code design, simulate and synthesize the following with a suitable FPGA.

1. 8 to 3 programmable priority encoder
2. Full Adder using structural modeling
3. Flip Flops(D,SR,T,JK)
4. 4 bit arbitrary Counter,4 bit binary up/down/up-down counter with synchronous reset, 4 bit Johnson counter, BCD counter
5. Sequential block to detect a sequence(say 11101) using appropriate FSM
6. 8 bit ripple carry adder and carry skip adder
7. 8 bit Carry Select Adder
8. Stepper Motor and DC motor Interface
9. DAC Interface

Using System Verilog code, simulate the following

10. Full Subtractor using structural modeling
11. Flip Flops(D,SR,T,JK)
12. 4-bit synchronous/asynchronous counters, synchronous arbitrary counters

References:

1. Peter J. Ashenden, “Digital Design: An Embedded Systems Approach using Verilog”, Elsevier, 2010.
2. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education, 2 010.
3. Stuart Sutherland, “RTL Modeling with System Verilog for Simulation and Synthesis: Using System Verilog for ASIC and FPGA Design”, 1st Edition, Create Space Independent Publishing Platform, 2017.

Course Outcomes (COs):

1. Design and model complex combinational circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
2. Enumerate complex sequential circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
3. Develop test benches to simulate combinational and sequential circuits.(POs: 1, 3, 4, 5)
4. Illustrate how the language infers hardware and helps to simulate and synthesize the digital system. (POs: 1, 3, 4, 5)
5. Implement and analyze the digital systems using FPGAs with respect to speed and area. (POs: 1, 3, 4, 5)

TECHNICAL SEMINAR – I

Course Code: MLC15 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Seminar: Research Methods
2. Seminar: Technical Report Writing
3. Source/Ideas for a Research Problem
4. Choosing Research Papers
5. Reading Research Papers
6. Summarizing Research Papers: Written
7. Presenting Research: Oral
8. **REVIEW – I**
9. Critiquing: Oral & Written
10. Detailed analysis of Block Diagrams: Written
11. Detailed Analysis of Block Diagrams: Oral
12. Proposing Technical Solutions: Written
13. Proposing Technical Solutions: Oral
14. **REVIEW – II**

Course Outcomes (COs):

1. Identify a technical problem by performing a comprehensive literature survey. (POs: 1, 2, 3, 4, 5)
2. Compare different solution methods presented in the literature for the technical problem identified. (POs: 1, 2, 3, 4, 5)
3. Predict the impact of various software tools and methods for the identified problem. (POs: 1, 2, 3, 4, 5)
4. Display initial simulation results, showing replication of existing approaches for the identified problem.(POs: 1, 2, 3, 4, 5)
5. Construct a technical block diagram that shows an optimized solution for the identified problem, with respect to existing literature. (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Introduction to area	**10**	No information about the specific technical details in the chosen area.	Some information about the area, but no clarity in internal details.	Clear presentation of the technical details, internal working, and rationale of design choices.		**CO1, CO2**
Literature Survey	**10**	Very few quality sources pertinent to the chosen technical area. No recent articles used.	Ample sources from recent past, but not from quality sources or with zero or very few citations.	Ample sources from quality journals and conferences recently published, and having abundant citations.		**CO1, CO2**
Problem Statement	**10**	No clear problem identified in chosen area.	Identification of problem area, but no knowledge of underlying technical details.	Clear identification of problem area, along with parameters having an influence on the performance.		**CO3**
Reproduction of Existing Results	**10**	No simulation results shown.	Individual blocks simulated, but no comprehensive simulation.	Complete and consistent reproduction of existing results using appropriate software tools.		**CO4**
Research Questions	**10**	No hypothesis proposed.	Hypothesis is not sound/practical, and not backed by technical arguments.	Sound and practical hypothesis proposed, along with supporting technical/intuitive arguments.		**CO5**
TOTAL MARKS AWARDED						

WIRELESS COMMUNICATIONS

Course Code: MLC21 **Credits: 4:0:0**

Prerequisites: Digital Communication **Contact Hours: 56**

Course Coordinator: Sarala S. M.

UNIT – I

Wireless Channel: Wireless channel as a linear time-varying system, Physical modeling for wireless channels, Input/output model of wireless channel, Time and frequency response, Statistical models, Reflection from a ground plane, Power decay with distance and shadowing

Point to Point Communication: Baseband equivalent channel model, Detection in Rayleigh fading channel, Repetition coding, Orthogonal Frequency Division Multiplexing.

UNIT – II

Diversity: Introduction, Micro-diversity, Macro-diversity and simulcast, Combination of Signals, Error Probability in fading channels with diversity reception, Transmit diversity

UNIT – III

Capacity of Wireless Channels: AWGN channel capacity, Linear time invariant Gaussian channels, Capacity of fading channels

UNIT – IV

Spatial Multiplexing for 5G Wireless Communications: Receive diversity, Spatial multiplexing and channel modeling, Multiplexing capability of MIMO channels, Physical modeling of MIMO channels, Modeling MIMO fading channels

UNIT – V

MIMO Capacity and Multiplexing Architectures: V-BLAST architecture, Fast fading MIMO channel, Receiver architectures – Linear de-correlator, Successive cancellation, Linear MMSE receiver, D-BLAST architecture.

References:

1. David Tse, P. Viswanath, “Fundamentals of Wireless Communication”, Cambridge University Press NewYork, USA, 2005.
2. Andreas F. Molisch, “Wireless Communications”, Wiley Publications, 2009.

3. William C Y Lee, “Mobile Communication Engineering Theory and Applications”, 2nd Edition, McGrawHill Education, 2008.

Course Outcomes (COs):

1. Define characteristics of wireless channel strength over time and frequency. (POs: 1, 3, 4)
2. Employ the concept of different diversity techniques to overcome the effect of small scale multi-path propagation. (POs: 1, 3, 4)
3. Demonstrate the impact of channel uncertainty on the performance of diversity combining schemes. (POs: 1, 3, 4)
4. Employ spatial multiplexing for MIMO channels. (POs: 1, 3, 4)
5. Discuss the performance of MIMO receiver architecture. (POs: 1, 3, 4)

ADVANCED EMBEDDED SYSTEMS

Course Code: MLC22 **Credits: 4:0:0**

Prerequisites: Microcontrollers **Contact Hours: 56**

Course Coordinator: Lakshmi Shrinivasan

UNIT – I

Introduction to Embedded System: Core of the embedded System, Memories**,** Communication Interface, Sensors and Actuators

Typical Embedded System: Washing Machine – Application specific ES, Automotive communication buses

Introduction to ARM Cortex–M Processors: Advantages of the Cortex M processors, Applications of the ARM Cortex–M processors, Resources for using ARM processors and ARM microcontrollers

Hardware Software Co-Design and Program Modeling: Fundamental issues in hardware software Co-design computational models in embedded design: Data Flow-Graph/Diagram (DFG) Model, Control Data Flow Graph/Diagram (CDFG), State machine model with examples, Sequential program model, concurrent/communicating process model, unified modeling language (WML) UML building blocks, UML tools, Hardware and software trade-offs typical embedded product design and development approach

UNIT – II

Technical Overview: ARM Cortex –M4: Processor type, Architecture, Block diagram, Memory system, Interrupt and exception support, Features of ARM Cortex–M4 processor

Low Power and System Control Features: Low power features, Using WFI and WFE instructions in programming

Fault Exceptions and Fault Handling: Overview of faults, Causes of faults, Enabling fault handlers, Fault status registers and fault address registers

UNIT – III

Architecture of ARM Cortex-M4: Introduction to the architecture, Programmer's model, Behavior of the application program status register (APSR), Memory system, Instruction set: Cortex–M4 specific instructions, Barrel shifter, Exceptions and interrupts, System control block

UNIT – IV

Real Time Operating System (RTOS) based Embedded System Design: Operating system basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Task Communication, Task Synchronization, Device Drivers, How to Choose an RTOS

UNIT – V

Embedded System Development Environment: Embedded firmware design approaches, Embedded firmware development languages, the Integrated Development Environment (IDE), Types of files generated on cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging, Target hardware debugging and boundary scan

References:

1. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3 and Cortex-M4 processors", Elsevier Ltd., 2014.
2. Shibu. K. V. "Introduction to Embedded Systems", Tata McGraw Hill Education Private Ltd., 2009.

Course Outcomes (COs):

1. Identify the basic building blocks and computational models in embedded systems. (POs: 1, 3, 4)
2. Develop programs using technical knowledge of ARM Cortex M4 for embedded system firmware development.(POs: 1, 3, 4)
3. Describe various architectural features and importance of ARM Cortex M4. (POs: 1, 3, 4)
4. Appreciate RTOS for real time embedded system design. (POs: 1, 2, 3, 4)
5. Interpret the importance of debugger tools for embedded system design and development.(POs: 1,2,3, 4)

ADVANCED EMBEDDED SYSTEMS LABORATORY

Course Code: MLCL23 **Credits: 0:0:1**

Prerequisites: Microcontrollers and OS **Contact Hours: 28**

Course Coordinator: Lakshmi Shrinivasan

LIST OF EXPERIMENTS

Introduction to IDE of ARM Cortex M4

1. Assembly language data transfer programs
2. Factorial of a number generation, largest/smallest number from an given array of N numbers
3. Parity checking (odd or even), Ascending/Descending order of given N numbers

Hardware Interfacing Experiments using ARM Cortex M4

4. Design and interface a DC motor speed control and measurement
5. Generation of Sine, triangular and square waveforms using Dual DAC
6. Design and interface a simple elevator system
7. Design and interface a stepper motor for following operations: rotate clockwise, anti-clockwise for defined degree of angle
8. Design and interface a simple 3x8 calculator type Keypad module
9. Show how an output interfaced hardware module could be controlled using relay
10. Conversion of a sine wave by ADC and reconstruction of the same by DAC

Programs based on RTOS concepts in Linux environment

11. Introduction to Linux commands and fork() function demo
12. Show IPC using Pipes and FIFO

Model the given embedded system using UML tool

13. Static and dynamic aspects of the system using basic Class and sequence diagram and generate code

References:

1. Joseph Yiu, “The Definitive Guide to ARM Cortex–M3 and Cortex–M4 Processors”, Elsevier Ltd., 2014.
2. Shibu K V, “Introduction to Embedded Systems”, Tata McGraw Hill Education Private Limited, 2009.

Course Outcomes (COs):

1. Use simulation and emulation IDE. (POs: 1, 5)
2. Know the assembly instructions of ARM Cortex M4 with the help of assembly code. (POs: 1, 3, 5)
3. Write, compile and debug RTOS based programs. (POs: 1, 3, 5)
4. Interface and communicate peripheral modules to ARM Cortex M4 microcontroller. (POs: 3, 4, 5)
5. Develop various UML diagrams and models for an embedded system. (POs: 1, 3, 5)

ADVANCED SIGNAL AND IMAGE PROCESSING LABORATORY

Course Code: MLCL24 **Credits: 0:0:1**

Prerequisites: Digital Signal Processing **Contact Hours: 28**

Course Coordinator(s): Maya V. Karki, K. Indira

LIST OF EXPERIMENTS

Programs on Adaptive Filters

1. Estimation of power spectrum of AR, MA and ARMA process
2. Design of lattice predictor of order p
3. Stationary system identification
4. Generation of spectrogram of speech signal
5. FIR filter model using RLS algorithm
6. FIR filter model using LMS algorithm

Programs on Image Processing

7. Reading and displaying images, applying transformation function: log transform, power law transform, histogram equalization
8. Smoothing and sharpening spatial filters
9. Point, line and edge detection, Boundary detection, Basic global thresholding, Otsu's method and Region based segmentation
10. Extracting region and boundaries, Chain code representation, Boundary reconstruction using Fourier Descriptor
11. Dilation and Erosion of an image using structuring element, Labeling connected components, Morphological reconstruction
12. Object recognition using minimum distance, Bayes classifier
13. Object recognition using feed forwardneural network classifier

References:

1. J. G. Proakis, D. G. Manolakis, "Digital Signal Processing", 4th Edition, Prentice Hall, 2006.
2. Rafael C Gonzalez, Richard E Woods, "Digital Image Processing using MATLAB", 2nd Edition, Tata McGraw Hill, 2012.

Course Outcomes (COs):

1. Estimation of power spectral density of random processes. (POs:1,4,5)
2. Design and develop FIR filter model using LMS and RLS algorithm. (POs:1,4,5)
3. Analyze various image pre-processing algorithms. (POs:1,4,5)
4. Apply segmentation algorithms to detect objects. (POs:1,4,5)
5. Develop object recognition algorithms using different classifiers. (POs:1,4,5)

TECHNICAL SEMINAR – II

Course Code: MLC25 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Detailed discussion of block diagrams
2. Setting up the Simulation environment
3. Simulation of Results
4. Reproduction of Simulation Results: Written
5. Presentation of Simulation Results: Oral
6. Proposing a Technical block diagram: Written
7. Proposing a Technical block diagram: Oral
8. **REVIEW – 1**
9. Design of Experiments
10. Design of Experiments
11. Presentation of Simulation Results: Written
12. Presentation of Simulation Results: Oral
13. Comprehensive report writing
14. **REVIEW – 2**

Course Outcomes (COs):

1. Present initial simulation results, replicating existing findings. (POs: 1, 2, 3, 4, 5)
2. Propose a technical block diagram with arguments for improved performance. (POs: 1, 2, 3, 4, 5)
3. Present the tools required for performing experiments, and justify their appropriateness. (POs: 1, 2, 3, 4, 5)
4. Discuss simulation results and optimized performance metrics. (POs: 1, 2, 3, 4, 5)
5. Discuss the advantages and disadvantages of approach, along with possible future directions.(POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Reproduction of existing results	**10**	Partial reproduction of results or large variation from reported results, no proper presentation using tables etc.	Partial reproduction of results, but no proper presentation and no analysis.	Complete reproduction of results, with appropriate tables/figures and analysis of results obtained.		**CO1**
Proposed Approach	**10**	No proper justification for methods used, or no new methods proposed.	New approach proposed, but without any justification.	New approach proposed, along with technical arguments that support the hypothesis.		**CO2**
Tool usage	**10**	Tool usage is not appropriate, is incorrect, or is incomplete.	Tools are used appropriately, but without knowledge of advanced options.	Tools are used appropriately, with complete knowledge of all available settings options suitable for analysis.		**CO3**
Results	**10**	Results are not indicative of proposed model, or are incomplete.	Results are complete, but are not better than existing solutions. Proper formats are used for presentation.	Results are presented using appropriate formats, and are better than existing solutions for the problem identified.		**CO4**
Discussion & Conclusions	**10**	No discussion of experiments and the results obtained.	Summary of experiments and results obtained thereby.	Summary of experiments and results obtained thereby, along with conclusions and future directions.		**CO5**
TOTAL MARKS AWARDED						

MULTIMEDIA COMMUNICATION

Course Code: MLC31 **Credits: 4:0:0**

Prerequisites: Digital Signal Processing **Contact Hours: 56**

Course Coordinator(s): Maya V. Karki

UNIT – I

Introduction to Multimedia: Introduction, Network and network services, Multimedia sources, Sources and destination services, Applications of multimedia communication networks: Video streaming to multiple users, Video conferencing

Multimedia Software Tools: Multimedia presentation, Editing and authoringtools in multimedia, Graphics and image data representation, Digital video, Video display interfaces

UNIT – II

Audio and Image Coding Standards: Architectural overview of audio standards, Psychoacoustic modeling, Time frequency mapping, Quantization, Variable length coding, MPEG audio coding standards, Image compression: Quantization, Transform coding: KLT, DCT and Wavelet transforms, EZW and SPIHT algorithm, Standards: JPEG, JPEG 2000

UNIT – III

Video Compression and Standards: Basic video compression techniques, Video compression based on motion compensation, Search for motion vectors, H.261, MPEG video coding:1,2,4 and 7, Video coding standards: H.264, H.265

UNIT –IV

Network Services and Protocols for Multimedia Communication: Local area networks and access Networks, Internet technologies and protocols, Multicast extension, Quality of Service for multimedia communication, Protocols for multimedia transmission and interaction

UNIT – V

Internet Multimedia Communication: Content multimedia distribution, Broadcast multicast Video-on-demand, Peer-to-peer video streaming with mesh overlays, HTTP based media streaming, Multimedia over wireless and mobile networks: 4G cellular networks and beyond, Multimedia cloud computing

References:

1. Ze Nian Li, Mark S Drew, Jiangchuan Liu, "Fundamentals of Multimedia", 2nd Edition, Springer, 2014.
2. Gerry D Gibson, "Multimedia Communications: Directions and Innovations", Academic Press, 2001.
3. Ranjan Parekh, "Principles of Multimedia", 2nd Edition Tata McGraw Hill, 2013.
4. Fred Halsall, "Multimedia Communications", 1st Edition, Pearson Education, 2011

Course Outcomes (COs):

1. Appraise basics of multimedia communication and multimedia software tools. (POs: 1, 3, 4)
2. Illustrate different audio and image coding standards. (POs: 1, 3, 4)
3. Elaborate on video compression based on motion compensation and MPEG video coding. (POs: 1, 3, 4)
4. Appreciate various network services and protocols for multimedia communication. (POs: 1, 3, 4)
5. Employ internet technologies for multimedia content distribution. (POs: 1, 3, 4)

INTERNSHIP/INDUSTRIAL TRAINING

Course Code: MLC32 **Credits: 0:0:4**

Prerequisites: Nil

The evaluation of students will be based on an intermediate presentation, along with responses to a questionnaire testing for outcomes attained at the end of the internship. The rubrics for evaluation of the presentation and the questionnaire for the report will be distributed at the beginning of the internship.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels				CO Mapping
		Inadequate (0% – 33 %)	Developing (34% – 66%)	Proficient (67% – 100%)	Marks Awarded	
Complex Technical Blocks	**10**	No working knowledge of the domain.	Working knowledge of the domain, with some knowledge of internal details.	Detailed understanding of the system, along with underlying mechanisms.		**CO1**
Error Debugging	**10**	No ability to diagnose or correct errors, or improve performance.	An ability to diagnose errors, but not correct them, no intuition on improving performance.	Diagnose and correct erroneous system operation, and propose methods to improve system performance.		**CO2**
Professional and Ethical Behavior	**10**	No knowledge of the requirement of professional and ethical behavior.	Understands the requirement for professional and ethical behavior.	Can predict the effects of non-professional an un-ethical behavior in the workplace.		**CO3**
Engineering and Finance	**10**	Cannot make the connection between engineering decisions and their economic impact.	Predict the cost of engineering decisions.	Creates designs keeping their economic impact in mind.		**CO4**
Lifelong Learning	**10**	No understanding of the requirements for lifelong learning in the engineering profession.	Can present examples of the impact of lifelong learning in the engineering industry.	Can present examples of the impact of lifelong learning, along with predicting future areas of impact of life-long learning.		**CO5**
				TOTAL MARKS AWARDED		

Course Outcomes (COs):

1. Analyze the working of complex technical systems/blocks. (POs: 1, 3, 4)
2. Correct errors during functioning and improve the performance of complex technical systems/blocks. (POs: 1, 3, 4)
3. Understand the importance of professional and ethical behavior in the engineering workplace. (POs: 1, 3, 4)
4. Predict the effect of engineering decisions on financial matters. (POs: 1, 3, 4)
5. Appreciate the requirements for constant technology updation. (POs: 1, 3, 4)

PROJECT WORK – I

Course Code: MLC33 **Credits: 0:0:6**
Prerequisites: Nil

The students will be evaluated based on two oral presentations during the semester. In the presentations they will have to discuss the results of their literature survey and initial implementations of the design.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – I, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Introduction	**5**	Introduction is not clear, or is not technically accurate.	Introduction is accurate, but no in-depth analysis of the domain.	Clear introduction to the domain, along with design decisions and their impacts.		**CO1**
Literature survey	**10**	Few sources of low quality, with no proper discussion of results.	Appropriate discussion of existing results, but quality of sources is low.	Comprehensive list of results presented from recent quality sources.		**CO2**
Methods comparison	**5**	Methods not explained and compared in terms of internal implementation details.	Advantages and disadvantages discussed, but not with reference to actual methods.	Detailed description of existing methods, along with their advantages and disadvantages.		**CO3**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – I, Review – II				CO Mapping
		Inadequate (0% – 33 %)	Developing (34% – 66%)	Proficient (67% – 100%)	Marks Awarded	
Methods discussion	**10**	No implementation level discussion of methods used in literature.	Brief discussion of tools used and results obtained therein.	Detailed discussion of tools used and their impact on the quality of results obtained in literature sources.		**CO3**
Initial Results	**10**	Initial results are not complete, or do not match that of existing literature.	Proper tools used to generate results, but are not same as existing literature.	Suitable tools used with appropriate conditions to generate initial results, and a discussion of the latter.		**CO4**
Technical Block Diagram	**10**	Technical block diagram proposing improvements is not technically justified.	Block diagram proposing improvements is technically justified.	Multiple block diagrams for optimization are presented, with a detailed analysis of the advantages and disadvantages of each approach.		**CO5**
				TOTAL MARKS AWARDED		

Course Outcomes (COs):

1. Introduce the technical area chosen and demonstrate that the focus of the study is on a significant problem worth investigation. (POs: 1, 3, 4, 5)
2. Discuss existing/standard solution strategies for the problem identified and its deficiency in the current scenario. (POs: 1, 2, 3, 4, 5)
3. Compare and contrast various research outcomes as part of a literature survey of quality published academic work. (POs: 1, 3, 4, 5)
4. Replicate existing results by choosing appropriate tools/methods. (POs: 1, 3, 4, 5)
5. Present a technical block diagram and justify its improved performance, with respect to existing methods, through technical arguments. (POs: 1, 2, 3, 4, 5)

PROJECT WORK – II

Course Code: MLC41 **Credits: 0:0:22**
Prerequisites: Nil

The students will be evaluated based on two oral presentations, in which they will present their proposed solutions to the problem identified, and discuss the implementation details and results obtained.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – II, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Technical Block Diagram	**10**	A discussion of methods for optimization is not based on technical arguments.	One or more block diagrams presented for optimization, but not justified with technical arguments.	One or more block diagrams presented for optimization, along with along with accurate technical arguments for justification.		**CO1**
Initial Results	**10**	Results are not matching expectations, or are not complete.	Complete results generated, but not an improvement on existing metrics.	Complete results generated with an improvement over existing approaches due to proposed block diagram.		**CO2**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – II, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Design of Experiments	**10**	Few experiments conducted, with no relation to problem domain.	Significant experiments conducted, but with no structure and relation to problem domain.	Significant experiments conducted, with all relevant parameters being tested in an orderly manner, and with relevance to hypothesis.		**CO3**
Experimental Results	**10**	Few results, not covering all cases, and not optimizing performance.	Performance is moderately optimized with respect to existing approaches, but not to the level predicted by block diagram.	Significant improvement in results, matching predictions in technical block diagram.		**CO4**
Discussion & Future work	**10**	No qualitative or quantitative discussion of the method, and its key characteristics.	Method is discussed, but without arguments justifying the advantages and disadvantages of the approach.	Method is summarized in detail, along with technical arguments justifying the advantages and disadvantages of the proposed method.		**CO5**
				TOTAL MARKS AWARDED		

Course Outcomes (COs):

1. Present different methods for improving existing performance metrics with respect to existing literature, along with justified technical arguments. (POs: 1, 2, 3, 4, 5)
2. Implement solutions proposed using appropriate software tools. (POs: 1, 3, 4, 5)
3. Compare implemented solutions and choose the best possible option based on factors such as societal impact, cost, speed, and practicality. (POs: 1, 3, 4, 5)
4. Perform extensive experimentation to prove hypothesis. (POs: 1, 3, 4, 5)
5. Discuss the proposed methods pros and cons, and its applicability in different situations, along with scope for improvement. (POs: 1, 2, 3, 4, 5)

ELECTIVES

ANTENNA THEORY AND DESIGN

Course Code: MLCE01 **Credits: 4:0:0**

Prerequisites: Field Theory and Microwave Circuits **Contact Hours: 56**

Course Coordinator: Sujatha B

UNIT – I

Antenna Fundamentals and Definitions: Radiation patterns, Directivity and gain, Effective height and aperture, Antenna impedance, Radiation efficiency, Antenna polarization

Arrays: Array factor for linear arrays, uniformly excited equally spaced linear arrays, Pattern multiplication, Directivity of linear arrays, Multidimensional arrays and feeding techniques

UNIT – II

Resonant Antennas: Dipole antenna – Far field electric and magnetic field components, Radiation resistance, Yagi-Uda antenna

Broadband Antennas: Travelling wave wire antennas, Helical antennas – Normal mode helix antenna, Axial mode helix antenna, Bi-conical antennas, Sleeve antenna

UNIT – III

Frequency Independent Antennas: Principle of frequency independent antennas, Log-periodic antennas

Microstrip and Printed Antennas: Feeding methods, Rectangular patch, Circular patch, Resonant frequencies and design, Quality factor, Bandwidth and efficiency

UNIT – IV

Aperture Antennas: Techniques for evaluating gain, Pyramidal horn antenna, Reflector antennas – Parabolic reflector antenna principles, Axi-symmetric parabolic reflector antenna, Offset parabolic reflectors, Dual reflector antennas, Gain calculations for reflector antennas, Feed antennas for reflectors, Field representations, Matching the feed to the reflector, General feed model, Feed antennas used in practice

UNIT – V

Antenna Array Synthesis: Formulation of the synthesis problem, Synthesis principles, Line sources shaped beam synthesis, Linear array shaped beam synthesis, Comparison of shaped beam synthesis methods, Low side lobe narrow main beam synthesis methods, Dolph Chebyshev linear array

Computational Electromagnetics (CEM) for antennas: Introduction to CEM, Methods of moments, Pocklington's integral equation, Integral equation and Kirchhoff's networking equations, Source modeling weighted residual formulations

References:

1. Warren L. Stutzman, Gary A. Thiele, "Antenna Theory and Design", 2nd Edition, John Wiley and Sons, 2012.
2. Constantine. A. Balanis, "Antenna Theory Analysis and Design", 3rdEdition, John Wiley, 2016.
3. John D Kraus, Ronald J Marhefka, Ahmad S Khan, "Antennas", 4thEdition, Tata McGraw Hill, 2006.

Course Outcomes (COs):

1. Define the parameters of antenna and analyze the uniform excited array antennas. (POs: 1, 3, 4)
2. Design the resonant and broad band antennas. (POs: 1, 3, 4)
3. Apply different feeding techniques and design microstrip patch antennas. (POs: 1, 3, 4)
4. Design the directivity and gain of parabolic reflector and explain the feed methods of reflector antennas. (POs: 1, 3, 4)
5. Synthesize antenna beam pattern using different types of distributions and describe the computationally efficient approximations using MOM. (POs: 1, 3, 4)

DIGITAL SYSTEM DESIGN USING HDL

Course Code: MLCE02 **Credits: 4:0:0**

Pre-requisites: Digital Electronics **Contact Hours: 56**

Course Coordinator: Gangadharaiah S L

UNIT – I

Introduction and Methodology: Digital and embedded Systems, Binary representation and circuit elements, Real world circuits, Models, Design methodology

Number Basics: Unsigned and signed integers, Fixed and floating-point numbers

UNIT – II

Sequential Basics: Storage elements, Counters, Sequential data paths and control, Clocked synchronous timing methodology

UNIT – III

Memories and Implementation Fabrics: Concepts, Memory types, Error detection and correction

Implementation Fabrics: ICs, PLDs, Packaging and circuit boards, Interconnection and signal integrity

UNIT – IV

System Verilog Simulation and Synthesis: System Verilog extension to Verilog, RTL and gate level modeling, RTL Synthesis, Subset of System Verilog, System Verilog simulation, Digital synthesis, Modules, Procedural blocks

UNIT – V

RTL Modeling Fundamentals: System Verilog language rules, module, module instances, Hierarchy, Four state data values, Data types, Variable types, Net types, Operators, Continuous signal assignments, Procedural signal assignments, Modeling combinational logic and sequential logic

References:

1. Peter J. Ashenden “Digital Design: An Embedded Systems Approach using Verilog”, Elsevier, 2010.
2. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, 2nd Edition, Pearson Education, 2010.
3. Stuart Sutherland, “RTL Modeling with System Verilog for Simulation and Synthesis: using System Verilog for ASIC and FPGA Design”, 1st Edition, Create Space Independent Publishing Platform, 2017.
4. Chris Spear, Greogory J Tumbush, “System Verilog for Verification: A Guide to Learning Test Bench Language Features”, Springer, 2012.

Course Outcomes (COs):

1. Apply the concepts of Verilog modeling to design and verify the operations of complex digital logic circuits.(POs:1, 3, 4)
2. Design and test pipelined storage elements, sequential data path controllers using Verilog (POs: 1, 3, 4)
3. Apply the concept of Verilog modeling to multi-port memories, FIFO data paths and FSMs with respect to integrated circuits. (POs:1,3,4)
4. Employ System Verilog to simulate and synthesize digital systems.(POs:1,3,4)
5. Model combinational and sequential circuits using System Verilog.(POs:1,3,4)

VLSI CIRCUITS AND SYSTEMS

Course Code: MLCE03 **Credits: 4:0:0**

Pre requisites: Digital Design **Contact Hours: 56**

Course Coordinator: V Anandi

UNIT – I

MOS Transistor Theory: n MOS/p MOS transistor, Threshold voltage equation, Body effect, MOS device design equation, Sub-threshold region, Channel length modulation, Mobility variation, Tunneling, Punch through, Hot electron effect MOS models, Small signal AC characteristics, CMOS inverter, βn/βp ratio, Noise margin, Static load MOS inverters, Transmission gate, Tristate inverter

UNIT – II

Circuit Characterization and Performance Estimation: Delay estimation – transient response, RC delay model, Elmore delay model, Linear delay model, Sizing with the method of logical effort

Combinational and Sequential Circuit Design: Static CMOS, CMOS circuit design families: CVSL, Pseudo nMOS, Pass transistor circuits, Sequential circuits: Circuit design of latches and flip-flops

UNIT – III

Data Path Sub System Design: Introduction, Addition – Carry lookahead, Carry Select, Tree Adders – Brent Kung, Kogge Stone, Sklansky, Subtraction, Multiplication: Carry-Save format, Booth algorithm, Comparators, Counters, Boolean logical operations, Coding, Shifters

UNIT – IV

Dynamic CMOS and Clocking: Introduction, Advantages of CMOS over NMOS, CMOS/SOS technology, CMOS/bulk technology, Latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking – Clock generation, clock distribution, clocked storage elements

UNIT – V

Timing Issues in Digital Circuits: Timing classification of digital systems, Synchronous design – Timing basics, Skew and Jitter, Latch based techniques, Self-timed circuits, Synchronization and Arbiters

References:

1. Neil H E Weste, David Harris, "CMOS VLSI Design: A System Perspective", 4th Edition, Pearson Education, 2014.
2. Jan M Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated circuits: A design perspective" 2nd Edition, Pearson Education, 2016.
3. Wayne Wolf, "Modern VLSI Design: System on Silicon", 3rd Edition, PHI, 2008.
4. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI, 3rd Edition, 2009.
5. Sung Mo Kang, Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw Hill, 3rdEdition, 2003.

Course Outcomes (COs):

1. Recall basics of CMOS digital integrated circuits. (POs:1, 3, 4)
2. Employ different performance metrics to predict the performance of VLSI circuits. (POs:1, 3, 4)
3. Apply digital design concepts to demonstrate different data path functions. (POs: 1, 3, 4)
4. Design and analyze dynamic CMOS circuits. (POs: 1, 3, 4)
5. Analyse variations in clock signals, and design circuits to reduce effects of large clock distribution networks. (POs: 1, 3, 4)

ADVANCED SIGNAL AND IMAGE PROCESSING

Course Code: MLCE04 **Credits: 4:0:0**

Pre requisites: Digital Signal Processing **Contact Hours: 56**

Course Coordinator: Maya V Karki

UNIT – I

Linear Prediction & Optimum Linear Filters: Random signals, Correlation functions and Power Spectra, Innovations representation of a stationary random process, Forward and backward linear prediction, Solution of normal equations, Properties of linear prediction – Error filters, Lattice and ARMA Lattice-Ladder Filters, Wiener filters for filtering and prediction

UNIT – II

Adaptive filters: Applications of adaptive filters, Linear Predictive Coding (LPC) of speech signal, Adaptive direct form FIR filters, LMS algorithm, Adaptive direct form filters, RLS algorithm

UNIT – III

Image Pre-processing: Basic intensity transformations, Histogram processing, Smoothing and sharpening spatial filters, Segmentation: Point, line and edge detection, Thresholding, Region based segmentation

UNIT – IV

Representation and Morphological Image processing: Representation: Chain codes, signatures, Boundary segments, Image boundary descriptors: Some simple descriptors and Fourier descriptor

Morphological Image Processing: Erosion and dilation, Basic morphological algorithms: Boundary extraction, hole filling extraction of connected components, Thinning, Thickening, skeletons, Morphological reconstruction

UNIT – V

Object Recognition: Patterns and pattern classification. Recognition based on decision theoretic methods: matching, Optimum statistical classifiers, Neural networks. Structural Methods: Matching shape numbers, String matching

References:

1. John G Proakis, Dimitris G Manolakis, “Digital Signal Processing”, 4th Edition, Prentice Hall, 2006.
2. Rafael C Gonzalez, Richard E Woods, “Digital Image Processing”, 3rd Edition, Pearson Education, 2009.
3. Milan Sonka, Vaclav Hlavac, Roger Boyle, “Image Processing, Analysis, and Machine Vision”, Cengage Learning, 2013.

Course Outcomes (COs):

1. Design linear predictors and optimum linear filters. (POs: 1,3,4)
2. Design adaptive filters with LMS and RLS algorithms. (POs: 1,3,4)
3. Apply segmentation algorithms to detect and link edges in an image. (POs: 1,3,4)
4. Represent and apply morphological algorithms to describe the shape and characteristics of an object. (POs: 1,3,4)
5. Apply different object recognition algorithms to detect objects in a scene. (POs:1,3,4)

MEMS AND NANOELECTRONICS

Course Code: MLCE05 **Credits: 4:0:0**

Prerequisites: Semiconductor Theory **Contact Hours: 56**

Course Coordinator: Lakshmi S

UNIT – I

Introduction to MEMS: Feynman's vision, Multi-disciplinary aspects, Application areas, Scaling laws in miniaturization, Scaling in geometry, scaling in rigid body dynamics, Electrostatics, Electromagnetics, Electrical, fluid flow.

Micro and Smart Devices and Systems – Principles: Transduction principles in MEMS Sensors: Actuators: different actuation mechanisms –Silicon capacitive accelerometer, Piezo-resistive pressure sensor, Blood analyzer, Conductometric gas sensor, Silicon micro-mirror arrays, Piezo-electric based inkjet print head, Electrostatic comb-driver

UNIT – II

Micro Manufacturing and Packaging: Lithography, Thin-film deposition, Etching (wet and dry), etch stop techniques, Wafer-bonding, Silicon micromachining: surface, bulk, LIGA process.

Integration and Packaging of MEMS Devices: Integration of microelectronics and micro devices at wafer and chip levels, Microelectronic packaging: wire and ball bonding, flip chip.

UNIT – III

Electrical and Electronic Aspects of MEMS: Coupled electro mechanics, Stability and Pull-in phenomenon, Practical signal conditioning circuits for microsystems, RF MEMS: Switches, varactors, tuned filters

UNIT – IV

Introduction to Nanoelectronics: Particles and waves, Wave-particle duality, Wave mechanics, Schrödinger wave equation, Materials for nanoelectronics, Semiconductors, Crystal lattices: Bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched and pseudomorphic heterostructures, Inorganic-organic heterostructures, Carbon nanomaterials: nanotubes and fullerenes

Electron Transport in Nanostructures: Electrons in traditional low-dimensional structures, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots, Nanostructure devices, Resonant-tunneling diodes, Single-electron-transfer devices, Nano-electromechanical system devices, Quantum-dot cellular automata.

UNIT – V

Fabrication, Measurement and Applications: Fabrication and measurement techniques for nanostructures, Bulk crystal and heterostructure growth, Nanolithography, etching, other means for fabrication of nanostructures and nanodevices, Techniques for characterization of nanostructures, Spontaneous formation and ordering of nanostructures, Clusters and nanocrystals

Applications: Injection Lasers: Quantum cascade lasers, Single photon sources, Biological tagging, Optical memories, Coulomb blockade devices, Photonic structures, QWIPs, NEMS, and MEMS

References:

1. G .K.Ananthasuresh, K.J.Vinoy, S. Gopalakrishnan, K.N.Bhat, V.K.Aatre, "Micro and Smart Systems", 1st Edition, Wiley India, 2010.
2. T R Hsu, "MEMS and Microsystems Design and Manufacturing", 2nd Edition, Tata McGraw Hill, 2008.
3. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press, 2011.
4. George W. Hanson, "Fundamentals of Nanoelectronics", Pearson Education India, 2009.

Course Outcomes (COs):

1. Analyze scaling laws and operation of various practical MEMS. (POs: 1,3)
2. Describe various fabrication techniques and packaging methods for MEMS devices. (POs: 1, 3)
3. Identify the electronics and RF aspects of MEMS. (POs: 3,4)
4. Recognize the distinguishing aspect of nanoscale devices and systems. (POs: 3, 4)
5. Examine design, fabrication and characterizationof nanoscale systems and their applications. (POs: 3, 4)

MACHINE & DEEP LEARNING

Course Code: MLCE06 **Credits: 4:0:0**

Prerequisites: Advanced Engineering Mathematics **Contact Hours: 56**

Course Coordinator: S. Sethu Selvi

UNIT – I

Introduction: What is machine learning, Example machine learning applications

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization

Bayesian Decision Theory: Classification, Losses and Risks, Discriminant functions, Association rules

UNIT – II

Parametric Methods: Maximum likelihood estimation, Evaluating an estimator, Bayes estimator, Parametric classification, Regression, Tuning model capacity

Dimensionality Reduction: Subset Selection, Principal Component Analysis (PCA), SVD and Matrix factorization, Linear Discriminant Analysis (LDA)

UNIT – III

Unsupervised Learning: Clustering:k–Means Clustering, EM algorithm, Hierarchical Clustering, Decision Trees: Univariate and Multivariate trees

UNIT – IV

Multilayer Perceptrons: Perceptron, Training a perceptron, Learning Boolean functions, Multilayer perceptrons, Backpropagation algorithm, Training procedures, Dimensionality reduction, Deep learning

Deep Neural Networks: Deep feed forward networks, regularization for deep learning

UNIT – V

Deep Neural Networks: Optimization for training deep models, convolutional networks

Sequence Modeling: Recurrent and Recursive nets, LSTM, Gated RNNs, Practical methodology, Applications

References:

1. Ethem Alpaydin, “Introduction to Machine Learning”, 3rd Edition, PHI Learning Pvt. Ltd, 2015.
2. Ian Goodfellow, YoshuaBengio, Aaron Courville, “Deep Learning”, MIT Press, 2017.
3. Christopher Bishop, “Pattern Recognition and Machine Learning”, CBS Publishers & Distributors, 2010
4. Tom Mitchell, “Machine Learning”, McGraw Hill, 1997.
5. Michael Nielsen, “Neural Networks and Deep Learning”, 2019.

Course Outcomes (COs):

1. Examine the concepts of various supervised learning algorithms and employ bayesian learning for classification (POs: 1, 3, 4)
2. Evaluate parametric methods for classification and investigate various dimensionality reduction algorithm (POs: 1, 3, 4)
3. Analyse unsupervised learning algorithms and multivariate concepts (POs: 1, 3, 4)
4. Appreciate the concepts of deep learning and apply deep feed forward network practical problems (POs: 1, 3, 4)
5. Apply convolutional networks and demonstrate how recurrent and recursive nets function can be mapped to practical applications (POs: 1, 3, 4)

INTERNET OF THINGS (IoT)

Course Code: MLCE07 **Credits: 4:0:0**

Prerequisites: Computer Networks **Contact Hours: 56**

Course Coordinator: Suma K V

UNIT – I

Introduction and Concepts: Definition and characteristics of IoT, Things in IoT, IoT protocols, IoT functional blocks, IoT communication models, IoT communication APIs, IoT enabling technologies, IoT levels and deployment templates, IoT and M2M, SDN and NFV for IoT, IoTsystem management with NETCONFIG – YANG

UNIT – II

Developing Internet of Things: IoT platform design methodology, Specifications: Requirements, Process, Domain, Information, Services, Level, Functional, Operational, Integration, Application development

Python Language: Data types anddata structures, Control flow, Functions, Modules, Packages, File handling, Date andtime operations, Classes, Python packages of interest for IoT

UNIT – III

IoT Physical Devices and End Points: Basic building blocks of an IoT Device, Raspberry Pi, Linux on Raspberry Pi, Raspberry Pi Interfaces: Serial, SPI, I2C

Programming Raspberry Pi with Python: Controlling LED, Interfacing switch, Interfacing light sensor

UNIT – IV

Cloud and Data Analytics: Introduction to cloud storage models and communication APIs

Web Application Framework: Django, Web services for IoT, Skynet messaging platform, Data analytics for IoT, Apache: Hadoop, Oozie, Storm, Real time data analysis, Tools for IoT

UNIT – V

IoT Case Studies: Home automation: Smart lighting, Home intrusion detection, Cities: Smart parking environment: Weather monitoring system, Weather reporting bot, Air pollution monitoring, Forest fire detection, Agriculture – Smart Irrigation, IoT printer, IoT in automobiles: Intelligent transportation and connected vehicles, Vehicular Ad-hoc Networks (VANETs)

References:

1. Arshdeep Bahga, Vijay Madisetti, “Internet of Things: A Hands-on Approach”, University Press, 2015.
2. Pethuru Raj, Anupama C Raman, “The Internet of things: Enabling Technologies, Platforms, and Use Cases Description”, Taylor & Francis, CRC Press, 2017.
3. Daniel Minoli, “Building the Internet of Things with IPv6”, John Wiley & Sons, 2013.

Course Outcomes (COs):

1. Describe the OSI Model for the IoT/M2M systems. (POs: 1,3)
2. Design and integrate various applications of IoT models. (POs: 1,3)
3. Acquire knowledge of basic blocks of IoT devices using Raspberry Pi. (POs:3)
4. Appreciate cloud storage models and web services for IoT. (POs: 3)
5. Appraise with various case studies on IoT. (POs: 1,3,4)

ADVANCED COMPUTER NETWORKS

Course Code: MLCE08 **Credits: 4:0:0**

Prerequisites: Computer Communication Networks **Contact Hours: 56**

Course Coordinator: Flory Francis

UNIT – I

Local Area Networks: Ethernet - Physical layer, MAC, LLC, LAN **i**nterconnection, Token ring, Physical layer, MAC, LLC, FDDI

Switching: Introduction, Circuit switching, Packet switching, Multicasting

Scheduling: Introduction, Requirements, Choices, Performance bounds, Best effort techniques, Naming and addressing

UNIT – II

Traffic Management: Introduction, Framework for traffic management, Traffic models, Traffic classes, Traffic scheduling

Control of Networks: Objectives and methods of control, Routing optimization in circuit and datagram networks, Markov chains, Queuing models in circuit and datagram networks

UNIT – III

Congestion and Flow control: Window congestion control, Rate congestion control, Control in ATM networks, Flow control model, Open loop flow control, Closed loop flow control

UNIT – IV

Cryptography: Introduction, Symmetric ciphers, Block cipher structure, DES, AES cipher, Principles of public key cryptosystems, RSA algorithm

UNIT – V

Hash Functions and Message Authentication: One way hash functions using symmetric block algorithms and public key algorithms, Message authentication codes, Hash functions, Digital signature algorithm

References:

1. J. Walrand and P. Varaya, “High Performance Communication Networks”, Harcourt Asia (Morgan Kaufmann), 2000
2. S. Keshav, “An Engineering Approach to Computer Networking”, Pearson Education, 1997.
3. Leon-Garcia, and I. Widjaja, “Communication Networks: Fundamental Concepts and Key Architectures”, TMH, 2000.
4. William Stallings, “Cryptography and Network Security: Principles and Practice”, 6th Edition, Pearson Education Inc., 2014.

Course Outcomes (COs):

1. Describe the basic networking, data switching and scheduling techniques of networks. (POs: 1, 3)
2. Analyze various network traffic management and control techniques. (POs: 1, 3,4)
3. Discuss congestion and flow control. (POs: 1, 3)
4. Appraise the working for symmetric and public key ciphers. (POs: 1, 3,4)
5. Illustrate the importance of hash functions and message authentication codes. (POs: 1, 3, 4)

ERROR CONTROL CODING

Course Code: MLCE09 **Credits: 4:0:0**

Prerequisites: Information Theory and Coding **Contact Hours: 56**

Course Coordinator: Chitra M

UNIT – I

Introduction to Algebra: Groups, Fields, Binary field arithmetic, Basic properties of GF(2^m),Construction of Galois Field GF(2^m) and its properties, Computation using Galois field GF(2^m) arithmetic, Vector spaces and matrices on Galois field

UNIT – II

Linear Block Codes: Generator and parity check matrices, Encoding circuits, Syndrome and error detection, Minimum distance considerations, Error detecting and error correcting capabilities, Standard array and syndrome decoding, decoding circuits, Hamming codes, Reed-Muller codes, (24,12) Golay codes, Product codes and interleaved codes, applications

UNIT – III

Cyclic Codes: Introduction, Generator and parity check polynomials, Encoding using multiplication circuits, Systematic cyclic codes – Encoding using feedback shift register circuits, Generator matrix for cyclic code, Syndrome computing and error detection, Meggitt decoder, Error trapping decoding, (23,12) Golay codes, Cyclic Hamming codes, Shortened cyclic codes

UNIT – IV

BCH Codes: Binary primitive BCH codes, Decoding procedures, Implementation of Galois field arithmetic, Implementation of error correction.

Non-binary BCH Codes: q-ary linear block codes, Primitive BCH codes over GF(q), Reed – Solomon codes, Decoding of non-binary BCH and RS codes: Berlekamp - Massey algorithm, Gorenstein – Zierler algorithm

UNIT – V

Majority Logic Decodable Codes: One step majority logic decoding, One step majority logic decodable codes, Two-step majority logic decoding, Multiple-step majority logic decoding

Convolutional codes: Encoding of convolutional codes, Structural properties, Distance properties, Viterbi decoding algorithm for decoding, Soft output Viterbi algorithm, Stack and Fano sequential decoding algorithms, Majority logic decoding, Introduction to LDPC codes, Geometrical structure of LDPC codes, EG-LDPC codes, PG-LDPC codes, Applications

References:

1. Shu Lin and Daniel J. Costello. Jr., "Error Control Coding", 2nd Edition, Pearson Education, Prentice Hall, 2014.
2. Todd K. Moon, "Error Correction Coding: Mathematical Methods and Algorithms", 1stEdition, Wiley Publications, 2005.

Course Outcomes (COs):

1. Apply properties of Galois field to groups, fields, vector space, row space and sub-spaces. (POs: 1, 3, 4)
2. Employ linear block codes, RM codes and Golay codes in error detection and correction. (POs: 1, 3, 4)
3. Demonstrate cyclic block codes, cyclic Hamming codes, shortened cyclic codes and (23, 12) Golay codes in error detection and correction. (POs: 1, 3, 4)
4. Illustrate BCH, RSand other q-ary coding and decoding algorithms. (POs: 1, 3, 4)
5. Describe convolutional encoders and Viterbi and stack algorithm based decoders. (POs: 1, 3, 4)

BROADBAND WIRELESS NETWORKS

Course Code: MLCE10 **Credits: 4:0:0**

Prerequisites: Computer Communication Networks **Contact Hours: 56**

Course Coordinator: Flory Francis

UNIT – I

WiMAX Genesis and Framework: IEEE 802.16 standard from 802.16-2004 to 802.16e, WiMAX forum, WiMAX forum working groups, WiMAX forum white papers, WiMAX products certification, WiMAX certified products, Predicted products and deployment evolution, Product types, Products and deployment timetable, Other 802.16 standards, Korean Cousin: WiBro

Protocol Layers and Topologies: Protocol layers of WiMAX, Convergence sub-layer (CS), Medium Access Control Common Part Sublayer (MAC CPS), Security sub-layer, Physical layer, Single Carrier (SC) and OFDM, Network management reference model, WiMAX topologies

UNIT – II

Frequency Utilization and System Profiles: Cellular concept, Sectorization, Cluster size considerations, Handover, WiMAX system profiles

WiMAX Physical Layer: OFDM transmission, Basic principle: Use the IFFT operator, Time domain and frequency domain OFDM considerations, OFDM symbol parameters, Physical Slot (PS), Peak-to-Average Power Ratio (PAPR), OFDMA and its variants, Subcarrier permutations in WiMAX OFDMA PHY.802.16 transmission chains

UNIT – III

WiMAX MAC and QoS: CS layer, MAC function and frames, MAC addresses and MAC frames, MAC header format, MAC sub-headers and special payloads, Fragmentation, Packing and Concatenation, Basic, Primary and Secondary management connections, User data and MAC management messages, TLV encoding in the 802.16 standard, TLV encoding sets, Automatic Repeat Request (ARQ), ARQ feedback format, Hybrid ARQ (HARQ), Scheduling and link adaptation

UNIT – IV

Multiple Access and Burst Profile: Duplexing – FDD,TDD mode, Transmission of downlink and uplink subframes, OFDM PHY uplink and downlink subframe, OFDMA PHY frame, frame duration, Preambles, Maps of multiple access: DL-MAP and UL-MAP, DL-MAP message, UL-

MAP message, OFDMA PHY UL and DL MAP messages, Burst profile usage: DCD message and DIUC Indicator, Burst profile selection thresholds, DCD (Downlink Channel Descriptor) message, Transmission of the DCD message, DIUC values, UCD (Uplink Channel Descriptor) message and UIUC indicator, Mesh frame, Network control subframe, Schedule control subframe

Uplink Bandwidth Allocation and Request Mechanisms: Types of uplink access grant request, Contention based focused bandwidth request in OFDM PHY

UNIT – V

Radio Resource Management: Radio engineering consideration for WiMAX systems, Radio resource management procedures, Advanced antenna technologies in WiMAX, Multicast Broadcast Services (MBS), Multi-BS access, MBS frame

WiMAX Architecture: Need for a standardized WiMAX, High-level architecture requirements, Network reference model, Network functionalities

References:

1. LoutfiNuyami, "WiMAX Technology for Broadband Access", John Wiley, 2007.
2. Yan Zhang, Hsia-Hwa Chen, "Mobile WiMAX", Aurobech Publications, 2008.

Course Outcomes (COs):

1. Identify the different protocols and topologies in wireless networks. (POs: 1,3)
2. Discuss cellular concepts and physical layer specifications of WiMAX. (POs: 1,3)
3. Describe the MAC layer responsibilities and its frame format. (POs:1,3)
4. Employ various multiple access techniques for efficient spectrum allocation and utilization. (POs:1,3)
5. Describe the functional blocks of WiMax architecture and RF resource management. (POs: 1,3)

COMMUNICATION SYSTEM DESIGN USING DSP

Course Code: MLCE11 **Credits: 4:0:0**

Prerequisites: Analog & Digital Communication **Contact Hours: 56**

Course Coordinator: T. D. Senthilkumar

UNIT – I

Introduction: Digital filters, Discrete time convolution and frequency responses, FIR filters – Using circular buffers to implement FIR filters in C and using DSP hardware, Interfacing C and assembly functions, Linear assembly code and the assembly optimizer. IIR filters – realization and implementation, FFT and power spectrum estimation: DTFT window function, DFT and IDFT, FFT, Using FFT to implement power spectrum

UNIT – II

Analog Modulation: Amplitude Modulation – Theory, generation and demodulation of AM, Spectrum of AM signal, Envelope detection and square law detection, Hilbert transform and complex envelope, DSP implementation of amplitude modulation and demodulation

DSBSC: Theory, Generation of DSBSC, Demodulation using coherent detection and Costas loop, Implementation of DSBSC using DSP hardware

SSB: Theory, SSB modulators, Coherent demodulator, Frequency translation, Implementation using DSP hardware

UNIT – III

Frequency Modulation: Theory, Single tone FM, Narrow band FM, FM bandwidth, FM demodulation, Discrimination and PLL methods, Implementation using DSP hardware

UNIT – IV

Digital Modulation: PRBS, and data scramblers: Generation of PRBS, Self-synchronizing data scramblers, Implementation of PRBS and data scramblers. RS-232C protocol and BER tester: The protocol, error rate for binary signaling on the Gaussian noise channels, Three bit error rate tester and implementation

UNIT – V

PAM: PAM theory, baseband pulse shaping and ISI, Implementation of transmit filter and interpolation filter bank. Simulation and theoretical exercises for PAM, Hardware exercises for PAM

QAM: Basic QAM transmitter, Constellation examples, QAM structures using passband shaping filters, Ideal QAM demodulation, QAM experiment. QAM receivers – Clock recovery and other frontend sub-systems, Equalizers and carrier recovery systems.

Experiment for QAM receiver frontend: Adaptive equalizer, Phase splitting, Fractionally spaced equalizer, Decision directed carrier tracking, Blind equalization, Complex cross coupled equalizer and carrier tracking experiment, Echo cancellation for full duplex modems: Multicarrier modulation, ADSL architecture, Components of simplified ADSL transmitter, a simplified ADSL receiver, Implementing simple ADSL transmitter and receiver

References:

1. Steven A. Tretter, "Communication System Design using DSP Algorithms with Laboratory Experiments for the TMS320C6713 DSK", Springer, 2008.
2. Vinay K Ingle, John G Proakis, "Digital Signal Processing using MATLAB", Cengage Learning, 2011.
3. John G. Proakis, MasoudSalehi, Gerhard Bauch, "Contemporary Communication Systems using MATLAB and Simulink", 2nd Edition, Thomson-Brooks/Cole, 2004.

Course Outcomes (COs):

1. Employ C and assembly functions in the implementation of filters and Fourier transforms, using DSP hardware. (POs: 1, 3, 4)
2. Apply amplitude modulation concepts in the DSP implementation of AM/DSB transceiver. (POs: 1, 3, 4)
3. Demonstrate the DSP hardware implementation of frequency modulation scheme. (POs: 1, 3, 4)
4. Analyze the bit error rate performance of the binary modulation receiver. (POs: 1, 3, 4)
5. Demonstrate the function of QAM transmitter and receiver hardware.(POs: 1, 3, 4)

RF AND MICROWAVE CIRCUIT DESIGN

Course Code: MLCE12 **Credits: 4:0:0**

Prerequisites: Microwave Circuits **Contact Hours: 56**

Course Coordinator: Sujatha B

UNIT – I

Wave Propagation in Networks: Introduction, Reasons for using RF/Microwaves, Applications, RF waves, RF and Microwave circuit design, Introduction to components basics, Analysis of simple circuit phasor domain, RF impedance matching, Properties of waves, transmission media, Micro strip lines, High frequency parameters, Formulation of S-parameters, Properties, transmission matrix, Generalized S-parameters

UNIT – II

Passive Circuit Design: Introduction, Smith chart, Scales, Application of Smith chart, Design of matching networks, Definition of impedance matching, Matching using lumped and distributed elements

Considerations in Active Networks and Design of Amplifiers, Oscillators and Detectors: Stability consideration, Gain consideration, Noise consideration

UNIT – III

Linear and Non-linear Design: Introduction, Types of amplifier, Design of different types of amplifiers, Multi-stage small signal amplifiers

Design of Transistor Oscillators: Oscillator versus Amplifier design. Oscillation conditions, Design of transistor oscillators, Generator tuning networks

UNIT – IV

RF/Microwave Frequency Conversion I: Rectifier and Detector Design: Detector losses, Effect of matching network on voltage sensitivity, Detector design

RF/Microwave Frequency Conversion II: Mixer Design: Mixers, Mixer types, Conversionloss for SSB mixers, One-Diode (or Single-Ended) mixers, Two-Diode mixers, Four-diode mixers, Eight-Diode mixers

UNIT – V

RF/Microwave Control Circuit Design: Phase shifters, Digital phase shifters, Semiconductor phase shifters, PIN diode attenuators

RF and Microwave IC design, MICs, MIC materials, Types of MICs, Hybrid v/s monolithic MICs

References:

1. Matthew M. Radmanesh, "RF and Microwave Electronics Illustrated", Pearson Education, 2004.
2. Reinhold Ludwig, Pavel Bretchko, "RF Circuit Design Theory and Applications", Pearson Education, 2004.

Course Outcomes (COs):

1. Employ transmission line theory, S-parameters, and Smith chart for microwave circuit analysis. (POs: 3, 4)
2. Design passive microwave matching circuits (POs: 3, 4)
3. Design microwave amplifiers, oscillators, resonators and micro-strip circuits. (POs: 3, 4)
4. Discuss features of active high-frequency matching networks, detector and mixer devices. (POs: 3, 4)
5. Design microwave and hybrid ICs using MIC materials. (POs: 3, 4)

SIMULATION, MODELING AND ANALYSIS

Course Code: MLCE13 **Credits: 4:0:0**

Prerequisites: Advanced Engineering Mathematics **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Basic Simulation Modeling: Nature of simulation, System models, discrete event simulation, Single server simulation, Alternative approaches, other types of simulation

UNIT– II

Building Valid, Credible and Detailed Simulation Models: Techniques for increasing model validity and credibility, comparing real world observations

UNIT – III

Selecting Input Probability Distributions: Useful probability distributions, Assessing sample independence, Activity – I, II and III, Model of arrival process

UNIT – IV

Random Number Generators: Linear congruential, Testing number generators, Random variate generation: Approaches, Continuous random variates, discrete random variates, correlated random variates

UNIT – V

Output Data Analysis: Statistical analysis for term initiating simulation, Analysis for steady state parameters, Comparing alternative system configuration, Confidence interval, Variance reduction techniques, Arithmetic and control variates

References:

1. Averill Law, "Simulation Modeling and Analysis", 4thEdition, McGraw Hill, 2007.
2. Jerry Banks, "Discrete Event System Simulation", Pearson Education, 2009.
3. Seila Ceric, Tadikamalla, "Applied Simulation Modeling", Cengage Publishing, 2009.
4. George. S. Fishman, "Discrete Event Simulation", Springer, 2001.
5. Frank L. Severance, "System Modeling and Simulation", Wiley, 2009.

Course Outcomes (COs):

1. Describe basic concepts in modeling and simulation. (POs: 1, 3,4)
2. Apply different techniques to increase model validity and credibility. (POs: 1, 3,4)
3. Choose different probability distributions for simulation and modeling. (POs: 1,3,4)
4. Apply random number variates to develop simulation models. (POs: 1,3, 4)
5. Analyze and test output data produced by the model. (POs: 1, 3, 4)

OPTICAL COMMUNICATION AND NETWORKING

Course Code: MLCE14 **Credits: 4:0:0**

Pre-requisites: Digital Communication **Contact Hours: 56**

Course Coordinator: M. Nagabushanam

UNIT – I

Introduction: Propagation of signals in optical fiber, Different losses, Nonlinear effects, Solitons, Optical sources, Detectors

Optical Components: Couplers, Isolators, Circulators, Multiplexers and filters, Gratings, Interferometers, Optical amplifiers

UNIT – II

Modulation and Demodulation: Signal formats, Ideal receivers, Practical detection receivers, Optical preamplifier, Noise considerations, Bit error rates, Coherent detection

UNIT – III

Transmission System Engineering: System model, Power penalty, Transmitter, Receiver, Different optical amplifiers, Dispersion

Optical Networks: Client layers of optical layer – SONET/SDH, Multiplexing, Layers, Frame structure, ATM functions, Adaptation layers, Quality of service and flow control, ESCON, HIPPI

UNIT – IV

WDM Network Elements: Optical line terminal optical line amplifiers, Optical cross connectors, WDM network design – cost trade-offs, LTD and RWA problems, Routing and wavelength assignment, Wavelength conversion

UNIT – V

Control and Management: Network management functions, Management framework, Information model, Management protocols, Layers within optical layer performance and fault management, Impact of transparency

References:

1. Rajiv Ramswami, K. N. Sivarajan, H.Sasaki, "Optical Networks", 3rd Edition, Morgan Kaufman Publishers, 2010.
2. John M. Senior, "Optical Fiber Communications: Principles & Practice", 3rd Edition, Pearson Education, 2009.
3. Gerd Keiser, "Optical Fiber Communication", 3rd Edition, McGraw-Hill, 2000.
4. Govind. P. Agarwal, "Fiber Optic Communication Systems", 3rd Edition, John Wiley, 2002.

Course Outcomes (COs):

1. Demonstrate the function of optical components and light propagation mechanism. (POs: 1, 3, 4)
2. Analyze the noise performance in optical communication receivers. (POs: 1, 3, 4)
3. Define signal impairment in optical networks. (POs: 1, 3, 4)
4. Demonstrate the principle of WDM network elements. (POs: 1, 3, 4)
5. Appreciate different network and management protocols in optical networks. (POs: 1, 3, 4)

SOFTWARE DEFINED RADIO

Course Code: MLCE15 **Credits: 4:0:0**

Prerequisites: Wireless Communication **Contact Hours: 56**

Course Coordinator: T. D. Senthilkumar

UNIT – I

Introduction to Software Radio Concepts: Characteristics, benefits and design principles of a software radio

Radio Frequency Implementation Issues: Purpose of RF front-end, Challenges of receiver design, RF receiver front-end topologies, RF components, Transmitter architecture, Noise and distortion in the RF chain, ADC and DAC conversion

UNIT – II

Multirate Signal Processing: Sample rate conversion principles, Poly phase filters, Digital filter banks, Timing recovery in digital receivers using digital filters

UNIT – III

Digital Generation of Signals: Introduction – Approaches to direct digital synthesis, Analysis of spurious signals, Band pass signal generation, Performance of direct digital synthesis system, Hybrid DDS-PLL systems, Generation of random sequences, ROM compression techniques

UNIT – IV

ADC and DAC: Introduction, Parameters of ideal and practical data converters – Sampling process, Quantization, Physical model, Transfer characteristics, Dynamic range, Timing issues, Analog bandwidth, Power consumption, Impact of noise and interference, Techniques to improve data converter performance

UNIT – V

Digital Hardware: Introduction, Hardware elements, DSP processors – Core, Architectures, Addressing, Pipelining, Multiprocessing using real-time operating systems, Software design cycle, Maximizing performance, Field programmable gate arrays, Power management issues

References:

1. J. H. Reed, “Software Radio”, Prentice Hall, 2002.
2. Eugene Grayver, “Implementing Software Defined Radio”, Springer, 2013.
3. Joseph Mitola, “Software Radio Architecture”, 1st Edition, John Wiley & Sons, 2002.

Course Outcomes (COs):

1. Describe the characteristics and design issues of RF components. (POs: 1, 3, 4)
2. Employ the principles of sampling rate conversion in implementation of digital poly phase filters. (POs: 1, 3, 4)
3. Describe the techniques to generate digital signals for random sequences. (POs: 1, 3, 4)
4. Apply design principles of data converters to improve its performance. (POs: 1, 3, 4)
5. Appraise the use of DSP processors and FPGA in the implementation of SDR. (POs: 1, 3, 4)

ASIC DESIGN

Course Code: MLCE16 **Credits: 4:0:0**

Prerequisites: VLSI Circuits and Systems **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Introduction to ASICs: Full custom, Semi-custom and programmable ASICs, ASIC design flow, ASIC cell libraries

CMOS Logic: Datapath logic cells**:** Data path elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path operators, I/O cells

UNIT – II

ASIC Library Design: Logical effort: Predicting delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages

Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT3 logic modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX

UNIT – III

Programmable ASIC I/O Cells: Xilinx and Altera I/O Block

Low-level Design Entry: Schematic entry: Hierarchical design, Netlist screener

ASIC Construction: Physical Design, CAD Tools

Partitioning: Goals and objectives, Constructive partitioning, Iterative partitioning improvement, KL and look ahead algorithms

UNIT – IV

Floor Planning: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning, Clock planning

Placement: Goals and objectives, Min-cut placement algorithm, Iterative placement improvement, Physical design flow

UNIT – V

Routing: Global routing: Goals and objectives, Global routing methods, Back-annotation

Detailed Routing: Goals and objectives, Measurement of channel density, Left-Edge and Area-routing algorithms. Special routing, Circuit extraction and DRC

References:

1. M J S Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd Edition, Addison Wesley/Pearson Education, 2011.
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011.
4. Rakesh Chadha, J. Bhasker, "An ASIC Low Power Primer: Analysis, Techniques and Specification", Springer Publications, 2015.

Course Outcomes (COs):

1. Describe the concepts of ASIC design methodology, data path elements and FPGA architectures. (POs: 4)
2. Design data path elements for ASIC cell libraries and compute optimum path delay. (POs: 4)
3. Employ industry synthesis tools to achieve desired objectives. (POs: 1, 2, 3, 5)
4. Design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain physical design flow. (POs: 1, 3, 4)
5. Create floor plan including partition and routing using CAD algorithms. (POs: 4)

ADVANCED COMPUTER ARCHITECTURE

Course Code: MLCE17 **Credits: 4:0:0**

Prerequisites: Computer Organization **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Parallel Computer Models: State of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers grain size and latency

Program and Network Properties: Conditions of parallelism, Data and resource dependencies, Hardware and software parallelism, Program partitioning and scheduling

UNIT – II

Program Flow Mechanisms: Control flow v/s data flow, Comparisons of flow mechanisms, Performance metrics and measures, Data flow architecture, Demand driven mechanisms

Principles of Scalable Performance: Parallel processing applications, Speedup performance laws, Scalability analysis and approaches

UNIT – III

Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speedup model, Scalability analysis and approaches

Advanced Processors: Advanced processor technology, Instruction set architectures, CISC scalar processors, RISC scalar processors, Superscalar processors, VLIW architectures

UNIT – IV

Pipelining: Linear pipeline processor, Nonlinear pipeline processor, Instruction pipeline, Design mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch handling techniques, Branch prediction, Arithmetic pipeline design

Memory Hierarchy Design: Cache basics and cache performance, Reducing miss rate and miss penalty, Multilevel cache hierarchies, Main memory organization, design of memory hierarchies

UNIT – V

Multiprocessor Architectures: Symmetric shared memory architectures, Distributed shared memory architectures, Models of memory consistency, Scalable cache coherence, Design challenges of directory protocols, Memory based directory protocols, Cache based directory protocols. Cache coherence protocols (MSI, MESI, MOESI), Overview of directory based approaches

References:

1. Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", 1st Edition, Tata McGraw Hill, 2003.
2. Kai Hwang, Zu, "Scalable Parallel Computers Architecture" Tata McGraw Hill, 2003.
3. M.J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing, 2002.
4. D.A. Patterson, J.L. Hennessy, "Computer Architecture: A Quantitative Approach", Morgan Kauffmann,2012.

Course Outcomes (COs):

1. Illustrate contemporary computer architecture issues and techniques.(POs:1,2)
2. Discuss the role of parallelism in current and future architectures. (POs:3)
3. Analyze the behavior of a processor pipeline for various sequences of instructions. (POs: 3,4)
4. Apply concept of cache and virtual memory for high performance computer architecture. (POs: 1,3,5)
5. Compare different multi-processor architectures and cache coherence protocols. (PO:3)

VLSI SIGNAL PROCESSING

Course Code: MLCE18 **Credits: 4:0:0**

Prerequisites: Digital Signal Processing **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Introduction to DSP Systems: Typical DSP Algorithms, DSP application demands and scaled CMOS Technologies, Representation of DSP algorithms

Iteration Bounds: Data flow graph representations, Loop bound and Iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs

UNIT – II

Pipelining and Parallel Processing: Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power

Retiming: Definition and properties, Solving systems of inequalities, Retiming techniques

UNIT – III

Unfolding: An algorithm for unfolding, Properties of unfolding, Critical path, Unfolding and retiming, Application of unfolding

Folding: Folding transformation, Register minimization techniques, Register minimization in folded architectures

Fast Convolution: Cook-Toom algorithm, Winograd algorithm, Iterated convolution, cyclic convolution, Design of fast convolution algorithm by inspection

UNIT – IV

Algorithmic Strength Reduction Techniques: 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters. Look-Ahead pipelining in first order IIR filters, Lookahead pipelining with power-of-2decomposition, Clustered look-ahead pipelining, parallel processing for IIR Filters, Combined pipelining and parallel processing for IIR filter, Low power IIR filter design using pipelining and parallel processing

UNIT – V

Bit-level Arithmetic Architectures: Parallel multipliers with sign extension, parallel carry-ripple array multiplier, parallel carry-savearray multiplier, Baugh–Wooley Multiplier, Parallel multipliers with modified Booth recoding, Design of Lyon's bit-serial multipliers using Horner's rule, Bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed arithmetic

References:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems: Design and Implementation", Wiley Interscience, 2007.
2. U. Meyer Baese, "Digital Signal Processing with Field Programmable Gate Arrays", 2nd Edition, Springer, 2004.
3. Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, "FPGA based Implementation of Signal Processing Systems", John Wiley, 2008.
4. S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
6. Lars Wanhammar, "DSP Integrated Circuits", 1st Edition, Academic Press Series in Engineering, 1999.

Course Outcomes (COs):

1. Enumerate use of various DSP algorithms and their representation using block diagrams, signal flow graphs and data-flow graphs. (POs: 1,3,4)
2. Apply the concept of pipelining, retiming and parallel processing in design of high-speed low power applications. (POs: 1,3,4)
3. Employ unfolding, folding and fast convolution in the design of VLSI architecture. (POs: 1,3,4)
4. Illustrate algorithmic strength reduction techniques to VLSI implementation of filters. (POs: 1,3,4)
5. Compare bit level arithmetic architectures for VLSI implementation of various DSP applications. (POs:1,3,4)